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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,740	08/05/2003	Hea-Suk Jung	51876P367	8831

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,740	JUNG, HEA-SUK	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☒ Claim(s) 4-7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on August 05,2003.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (Pub. No. U.S. 2003/0030473).

Regarding claim 1, Lee discloses a delay locked loop (DLL) in semiconductor device (Figure 1), comprising:

an clock buffer (11,12) receiving an external clock signal (clk) and an inverted clock signal (/clk) and outputting first (fall_clk) and second internal clock signals (rise_clk) to be used in the DLL circuit [0002]; and

a variable clock divider (13) receiving the second internal signal (rise_clk) from internal clock signal have predetermined pulse width according to a control signal based on a column address strobe clock buffer and variably dividing second (CAS) latency, which is set according a frequency external clock signal, wherein the control signal is initially set have a first logic level and is enabled to second logic level when the CAS latency corresponds predetermined frequency [0005].

Regarding claim 2, Lee discloses a plurality of delay lines, each delay line having plurality of unit delay (Figure 1, 10);

a phase comparator (19) comparing phase between reference clock signal generated from the variable clock divider and a feedback signal;

a shift controller (18) for generating a shift right signal or a shift left signal according to a comparison signal outputted from the phase comparator;

a shift register (17) for adjusting amount of delay of the delay lines in response to the shift right signal or the shift left signal; and

a delay model (22) generating feedback signal compensating a time difference between the external clock signal and the internal clock difference [0005-0010].

Regarding claim 3, Lee discloses wherein the variable clock divider (Figure 3A) includes:

a first divider (CD6) for generating a first divided signal generating first pulse width and a first period by receiving the second internal clock signal;

a second divider (CD5) for generating a second divided signal having the first pulse width and second period and a third divided signal having second pulse width and the second period by receiving the first divided signal;

selector (CSL) for selectively outputting the second divided signal and the third divided signal response to the control signal;

third clock divider (CD4) for generating fourth divided clock signal having the first pulse width and third period or a fifth divided clock signal having the second pulse width and the third period as a reference clock signal by receiving the second divided signal and the third divided signal; and

an output driver (247) outputting an inverted reference clock signal into the delay lines.

Allowable Subject Matter

8. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-7 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Lee (Pub. U.S. Patent No. 2003/0030473), and others, does not teach the claimed invention having a first divider includes a inverter for inverting the second internal clock signal.

Conclusion

Regarding claims 1-3, the claimed inventions are very similarly with Kanou et al. (U.S. Patent No. 6,172,537).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER